EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Paul Kravetz on 5/5/2009.

The application has been amended as follows, beginning on the next page:

1. (previously presented) A processing apparatus comprising:

an internal circuit comprising:

a CPU executing programs, said CPU is supplied with a first clock and executes the programs synchronously with the supplied first clock, and,

at least one internal device having a predetermined function, and

a bus line extending internally of the internal circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the internal circuit and an address bus and a data bus transferring an address and data, respectively, wherein said internal circuit includes at least one internal memory as an internal device, the internal memory storing a program for determining ciphering patterns; and

an external circuit provided externally of the internal circuit and connected with the externally extending portion of said bus line and including at least one external device having a predetermined function, wherein said external circuit includes at least one external memory as an external device, wherein

said internal circuit further comprises a ciphering section interposed at an entrance to an external side of said internal circuit, and ciphering the address and the data on the bus line by the ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device, to thereby prevent illicit access to the internal memory via the external memory, said ciphering section is supplied with a second clock and performs ciphering synchronously with the supplied second clock and a clock supply section for supplying the second clock at a higher speed than a speed of the first clock supplied to said CPU, to said ciphering section, so that one of the ciphering patterns that is made by using a result of one of other ciphering patterns among the ciphering patterns can be employed.

2. (original) A processing apparatus according to claim 1, wherein

the ciphering patterns adopted by said ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

3. (original) An processing apparatus according to claim 1, wherein

said external circuit includes a plurality of external devices; and

said ciphering section performs ciphering using ciphering patterns according to said plurality of external devices, respectively.

4. (previously presented) A processing apparatus according to claim 1, wherein

the ciphering section of the internal circuit further comprises a bus interface that externally outputs data ciphered by the ciphering section when access to the external device is requested and externally outputs dummy data when access to the external device is not requested.

5. (cancelled)

6. (original) A processing apparatus according to claim 1, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit and determining a ciphering pattern of said ciphering section according to the constitution of said external circuit.

7. (original) A processing apparatus according to claim 1, wherein

said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

8. (currently amended) A processing apparatus according to claim 1, comprising:

a deciphering section connected to the externally extending portion of said bus line, and returning the ciphered address and the data on the bus fine ~~line~~ line to an

address and data which are not ciphered.

9. (original) A processing apparatus according to claim 1, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is carried out for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

10. (original) A processing apparatus according to claim 1, wherein

said ciphering section adopts a ciphering pattern in which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device, to thereby cipher the data.

11. (canceled)

12. (cancelled)

13. (canceled)

14. (canceled)

15. (canceled)

16. (canceled)

17. (canceled)

18. (original) A processing apparatus according to claim 1, wherein

said internal circuit holds a ciphering pattern adopted by said ciphering section;

the processing apparatus further comprises a tamper detection section detecting tamper; and

ciphering pattern destruction means for destroying the ciphering pattern held in said internal circuit in response to tamper detection made by said tamper detection section.

19. (canceled)

20. (previously presented) An integrated circuit constituted by mounting:

a CPU executing programs and is supplied with a first clock and executes the programs synchronously with the supplied first clock;

at least one internal device having a predetermined function, wherein at least one internal device is an internal memory, the internal memory storing a program for determining ciphering patterns;

a bus line extending internally of the integrated circuit and connecting said CPU to said internal device, the bus line comprising an externally extending portion extending externally of the integrated circuit and an address bus and a data bus, wherein at least one external device having a predetermined function is provided externally of integrated circuit and connected with the externally extending portion of the bus line, and the bus line transferring an address and data via the address bus and the data bus, respectively, wherein at least one external device is an external memory; and

a ciphering section interposed at an entrance to an external side of the integrated circuit, and ciphering the address and the data on the bus line by the ciphering patterns according to a plurality of regions divided from a space allotted to entirety of the at least one external device, to thereby prevent illicit access to the internal memory via the external memory, said ciphering section is supplied with a second clock and conducts ciphering synchronously with the supplied second clock and operates with the second clock at a higher speed than a speed of the first clock with which said CPU operates, so that one of the ciphering patterns that is made by using a result of one of other ciphering patterns among the ciphering patterns can be employed.

21. (original) An integrated circuit according to claim 20, wherein

the ciphering patterns adopted by the ciphering section include one ciphering pattern in which neither the address nor data is ciphered.

22. (original) An integrated circuit according to claim 20, wherein

in case where a plurality of external devices are provided externally of the

externally extending portion of said bus line, said ciphering section performs ciphering by the ciphering patterns according to said plurality of external devices, respectively.

23. (previously presented) An integrated circuit according to claim 20, wherein

the ciphering section of the internal circuit further comprises a bus interface that externally outputs data ciphered by the ciphering section when access to the external device is requested and externally outputs dummy data when access to the external device is not requested.

24. (cancelled)

25. (original) An integrated circuit according to claim 20, comprising:

ciphering pattern determination means for recognizing a constitution of said external circuit, and for determining a ciphering pattern of said ciphering section according to the constitution.

26. (original) An integrated circuit according to claim 20, wherein

said ciphering section ciphers the address and the data on said bus line by ciphering patterns according to the plurality of regions divided from the address space allotted to the entirety of said no less than one external device and according to application programs executed by said CPU.

27. (original) An integrated circuit according to claim 20, comprising:

ciphering pattern change means for changing a ciphering pattern whenever a predetermined initialization operation is performed, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

28. (original) An integrated circuit according to claim 20, wherein

said ciphering section ciphers the data by adopting a ciphering pattern in

which ciphered data is changed according to the address, for one of the plurality of regions divided from the address space allotted to the entirety of said at least one external device.

29. (canceled)
30. (canceled)
31. (canceled)
32. (canceled)
33. (canceled)
34. (canceled)
35. (canceled)
36. (canceled)

Allowable Subject Matter

Claims 1-4, 6-10, 18, 20-23, and 25-28 are allowed.

The following is an examiner's statement of reasons for allowance:

The closest prior art, Taguchi (US Patent Number 5,915,025), teaches an internal circuit comprising a CPU executing programs, said CPU is supplied with a first clock and executes the programs synchronously with the supplied first clock, at least one internal device having a predetermined function and a bus line extending internally of the internal circuit and connecting said CPU to said internal device the bus line comprising an externally extending portion extending externally of said internal circuit and transferring an address and data, wherein said

internal circuit includes at least one internal memory as an internal device, the internal circuit including selection means for determining ciphering patterns.

Taguchi further teaches an external circuit provided externally of the internal circuit and connected with the externally extending portion of said bus line and including at least one external device having a predetermined function, wherein said external circuit includes at least one external memory as an external device. Taguchi also taught that the internal circuit comprises a ciphering section interposed at an entrance to an external side of said internal circuit and ciphering the data on the bus line by ciphering patterns according to a plurality of regions divided from an address space allotted to entirety of said at least one external device.

However, Taguchi failed to disclose ciphering of the address, that the selection means included a program stored in internal memory for determining the ciphering patterns, using separate clocks with the encryption clock being set at a higher frequency than the processor clock, or that one of the ciphering patterns is made by using a result of one of other ciphering patterns among the ciphering patterns.

While the prior art does disclose these limitations individually, there is no teaching in the prior art which would reasonably suggest having a ciphering section supplied with a clock which is faster than the clock of the CPU, a program for determining ciphering patterns, one of the ciphering patterns being made by using a result of one of other ciphering patterns among the ciphering patterns, and the ciphering section encrypting and decrypting addresses and data on the external bus line using the ciphering patterns according to a plurality of regions divided from an address space allotted to the entirety of the external circuit, in the specific combination of limitations as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW T. HENNING whose telephone number is (571)272-3790. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew T Henning/
Examiner, Art Unit 2431